16-Bit 1 MSPS PulSAR™ Unipolar ADC with Reference

AD7653

FEATURES

Throughput:
- 1 MSPS (Warp mode)
- 800 kSPS (Normal mode)
- 666 kSPS (Impulse mode)

16-bit resolution
Analog input voltage range: 0 V to 2.5 V
No pipeline delay
Parallel and serial 5 V/3 V interface
SPI®/QSPI™/MICROWIRE™/DSP compatible
Single 5 V supply operation
Power dissipation
- 92 mW typ @ 666 kSPS, 138 µW @ 1 kSPS without REF
- 128 mW typ @ 1 MSPS with REF

48-lead LQFP and 48-lead LFCSP packages
Pin-to-pin compatible with PulSAR ADCs

APPLICATIONS

Data acquisition
Instrumentation
Digital signal processing
Spectrum analysis
Medical instruments
Battery-powered systems
Process control

GENERAL DESCRIPTION

The AD7653* is a 16-bit, 1 MSPS, charge redistribution SAR analog-to-digital converter that operates from a single 5 V power supply. The part contains a high speed 16-bit sampling ADC, internal conversion clock, internal reference, error correction circuits, and both serial and parallel system interface ports. It features a very high sampling rate mode (Warp), a fast mode (Normal) for asynchronous conversion rate applications, and a reduced power mode (Impulse) for low power applications where power is scaled with the throughput. The AD7653 is fabricated using Analog Devices' high performance, 0.6 micron CMOS process, with correspondingly low cost. It is available in a 48-lead LQFP and a tiny 48-lead LFCSP with operation specified from –40°C to +85°C.

*Patent Pending.

FUNCTIONAL BLOCK DIAGRAM

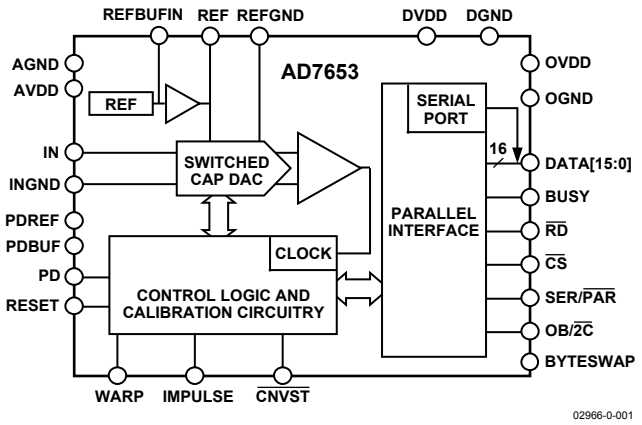

Figure 1.

Table 1. PulSAR Selection

Type/kSPS	100–250	500–570	800–1000
Pseudo-Differential	AD7651 AD7660/AD7661	AD7650/AD7652 AD7664/AD7666	AD7653 AD7667
True Bipolar	AD7663	AD7665	AD7671
True Differential	AD7675	AD7676	AD7677
18-Bit	AD7678	AD7679	AD7674
Multichannel/ Simultaneous		AD7654 AD7655	

PRODUCT HIGHLIGHTS

1. Fast Throughput.
   The AD7653 is a 1 MSPS, charge redistribution, 16-bit SAR ADC with internal error correction circuitry.

2. Internal Reference.
   The AD7653 has an internal reference with a typical temperature drift of 7 ppm/°C.

3. Single-Supply Operation.
   The AD7653 operates from a single 5 V supply. In Impulse mode, its power dissipation decreases with the throughput.

4. Serial or Parallel Interface.
   Versatile parallel or 2-wire serial interface arrangement is compatible with both 3 V and 5 V logic.

Rev. A

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SPECIFICATIONS

Table 2. –40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN} - V_{INGND}$	0		V_{REF}	V
Operating Input Voltage	V_{IN}	–0.1		+3	V
	V_{INGND}	–0.1		+0.5	V
Analog Input CMRR	f_{IN} = 10 kHz		65		dB
Input Current	1 MSPS Throughput		12		µA
Input Impedance[1]					
THROUGHPUT SPEED					
Complete Cycle	In Warp Mode			1	µs
Throughput Rate	In Warp Mode	1		1000	kSPS
Time between Conversions	In Warp Mode			1	ms
Complete Cycle	In Normal Mode			1.25	µs
Throughput Rate	In Normal Mode	0		800	kSPS
Complete Cycle	In Impulse Mode			1.5	µs
Throughput Rate	In Impulse Mode	0		666	kSPS
DC ACCURACY					
Integral Linearity Error		–6		+6	LSB[2]
No Missing Codes		15			Bits
Differential Linearity Error		–2		+3	LSB
Transition Noise			0.7		LSB
Unipolar Zero Error, T_{MIN} to T_{MAX}[3]				±25	LSB
Unipolar Zero Error Temperature Drift			±0.2		ppm/°C
Full-Scale Error, T_{MIN} to T_{MAX}[3]	REF = 2.5 V			±0.12	% of FSR
Full-Scale Error Temperature Drift			±0.4		ppm/°C
Power Supply Sensitivity	AVDD = 5 V ± 5%, with REF		±2		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 100 kHz		86		dB[4]
Spurious Free Dynamic Range	f_{IN} = 100 kHz		98		dB
Total Harmonic Distortion	f_{IN} = 45 kHz		–98		dB
	f_{IN} = 100 kHz		–96		dB
Signal-to-(Noise + Distortion)	f_{IN} = 100 kHz		86		dB
	–60 dB Input, f_{IN} = 100 kHz		30		dB
–3 dB Input Bandwidth			12		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			250	ns
REFERENCE					
Internal Reference Voltage	V_{REF} @ 25°C	2.48	2.50	2.52	V
Internal Reference Temperature Drift	–40°C to +85°C		±7		ppm/°C
Line Regulation	AVDD = 5 V ± 5%		±24		ppm/V
Turn-On Settling Time	C_{REF} = 10 µF		5		ms
Temperature Pin					
Voltage Output @ 25°C			300		mV
Temperature Sensitivity			1		mV/°C
Output Resistance			4.3		kΩ
External Reference Voltage Range		2.3	2.5	AVDD – 1.85	V
External Reference Current Drain	1 MSPS Throughput		300		µA

Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.8	V
V_{IH}		2.0		DVDD + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[5]					
Pipeline Delay[6]					
V_{OL}	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	OVDD − 0.6			V
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25[7]	V
Operating Current[8]	1 MSPS Throughput				
AVDD[9]	With Reference and Buffer		18.7		mA
AVDD[10]	Reference and Buffer Alone		3		mA
DVDD[11]			6.7		mA
OVDD[11]			200		µA
Power Dissipation without REF	666 kSPS Throughput[11]		92	115	mW
	1 kSPS Throughput[11]		138		µW
Power Dissipation with REF	1 MSPS Throughput[8]		128	145	mW
TEMPERATURE RANGE[12]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1]See Analog Input section.
[2]LSB means least significant bit. With the 0 V to 2.5 V input range, 1 LSB is 38.15 µV.
[3]See Definitions of Specifications section. These specifications do not include the error contribution from the external reference.
[4]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[5]Parallel or serial 16-bit.
[6]Conversion results are available immediately after completed conversion.
[7]The max should be the minimum of 5.25 V and DVDD + 0.3 V.
[8]In Warp mode.
[9]With REF, PDREF and PDBUF are LOW; without REF, PDREF and PDBUF are HIGH.
[10]With PDREF, PDBUF LOW and PD HIGH.
[11]Impulse Mode. Tested in Parallel Reading mode.
[12]Consult factory for extended temperature range.

TIMING SPECIFICATIONS

Table 3. −40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figure 26 and Figure 27					
Convert Pulse Width	t_1	10			ns
Time between Conversions (Warp Mode/Normal Mode/Impulse Mode)[1]	t_2	1/1.25/1.5			µs
$\overline{\text{CNVST}}$ LOW to BUSY HIGH Delay	t_3			35	ns
BUSY HIGH All Modes Except Master Serial Read after Convert					
(Warp Mode/Normal Mode/Impulse Mode)	t_4			0.75/1/1.25	µs
Aperture Delay	t_5		2		ns
End of Conversion to BUSY LOW Delay	t_6	10			ns
Conversion Time (Warp Mode/Normal Mode/Impulse Mode)	t_7			0.75/1/1.25	µs
Acquisition Time	t_8	250			ns
RESET Pulse Width	t_9	10			ns
Refer to Figure 28, Figure 29, and Figure 30 (Parallel Interface Modes)					
$\overline{\text{CNVST}}$ LOW to DATA Valid Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{10}			0.75/1/1.25	µs
DATA Valid to BUSY LOW Delay	t_{11}	12			ns
Bus Access Request to DATA Valid	t_{12}			45	ns
Bus Relinquish Time	t_{13}	5		15	ns
Refer to Figure 32 and Figure 33 (Master Serial Interface Modes)[2]					
$\overline{\text{CS}}$ LOW to SYNC Valid Delay	t_{14}			10	ns
$\overline{\text{CS}}$ LOW to Internal SCLK Valid Delay[2]	t_{15}			10	ns
$\overline{\text{CS}}$ LOW to SDOUT Delay	t_{16}			10	ns
$\overline{\text{CNVST}}$ LOW to SYNC Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{17}		25/275/525		ns
SYNC Asserted to SCLK First Edge Delay	t_{18}	3			ns
Internal SCLK Period[3]	t_{19}	25		40	ns
Internal SCLK HIGH[3]	t_{20}	12			ns
Internal SCLK LOW[3]	t_{21}	7			ns
SDOUT Valid Setup Time[3]	t_{22}	4			ns
SDOUT Valid Hold Time[3]	t_{23}	2			ns
SCLK Last Edge to SYNC Delay[3]	t_{24}	3			ns
$\overline{\text{CS}}$ HIGH to SYNC HI-Z	t_{25}			10	ns
$\overline{\text{CS}}$ HIGH to Internal SCLK HI-Z	t_{26}			10	ns
$\overline{\text{CS}}$ HIGH to SDOUT HI-Z	t_{27}			10	ns
BUSY HIGH in Master Serial Read after Convert[3]					
(Warp Mode/Normal Mode/Impulse Mode)	t_{28}		See Table 4		
$\overline{\text{CNVST}}$ LOW to SYNC Asserted Delay					
(Warp Mode/Normal Mode/Impulse Mode)	t_{29}		0.75/1/1.25		µs
SYNC Deasserted to BUSY LOW Delay	t_{30}		25		ns
Refer to Figure 34 and Figure 35 (Slave Serial Interface Modes)[2]					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	3		18	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	25			ns
External SCLK HIGH	t_{36}	10			ns
External SCLK LOW	t_{37}	10			ns

1In Warp mode only, the maximum time between conversions is 1 ms; otherwise, there is no required maximum time.
[2]In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.
[3]In Serial Master Read during Convert Mode. See Table 4 for Serial Master Read after Convert mode.

Table 4. Serial Clock Timings in Master Read after Convert

DIVSCLK[1] DIVSCLK[0]	Symbol	0 0	0 1	1 0	1 1	Unit
SYNC to SCLK First Edge Delay Minimum	t_{18}	3	17	17	17	ns
Internal SCLK Period Minimum	t_{19}	25	50	100	200	ns
Internal SCLK Period Maximum	t_{19}	40	70	140	280	ns
Internal SCLK HIGH Minimum	t_{20}	12	22	50	100	ns
Internal SCLK LOW Minimum	t_{21}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{22}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{23}	2	4	30	80	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	3	55	130	290	ns
BUSY HIGH Width Maximum (Warp)	t_{28}	1.5	2	3	5.25	µs
BUSY HIGH Width Maximum (Normal)	t_{28}	1.75	2.25	3.25	5.55	µs
BUSY HIGH Width Maximum (Impulse)	t_{28}	2	2.5	3.5	5.75	µs

DEFINITIONS OF SPECIFICATIONS

Integral Nonlinearity Error (INL)

Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Full-Scale Error

The last transition (from 011…10 to 011…11 in twos complement coding) should occur for an analog voltage 1½ LSB below the nominal full scale (2.49994278 V for the 0 V to 2.5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

Unipolar Zero Error

The first transition should occur at a level ½ LSB above analog ground (19.073 µV for the 0 V to 2.5 V range). Unipolar zero error is the deviation of the actual transition from that point.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to *S*/(*N*+*D*) by the following formula:

$$ENOB = (S/[N+D]dB - 1.76)/6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal, and is expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (S/[N+D])

S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

Aperture Delay

Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the AD7653 to achieve its rated accuracy after a full-scale step function is applied to its input.

Overvoltage Recovery

Overvoltage recovery is the time required for the ADC to recover to full accuracy after an analog input signal 150% of the full-scale value is reduced to 50% of the full-scale value.

Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is the change of internal reference voltage output voltage V over the operating temperature range and normalized by the output voltage at 25°C, expressed in ppm/°C. The equation follows:

$$TCV(ppm/°C) = \frac{V(T_2) - V(T_1)}{V(25°C) \times (T_2 - T_1)} \times 10^6$$

where:
$V(25°C) = V$ at +25°C
$V(T_2) = V$ at Temperature 2 (+85°C)
$V(T_1) = V$ at Temperature 1 (–40°C)

TYPICAL PERFORMANCE CHARACTERISTICS

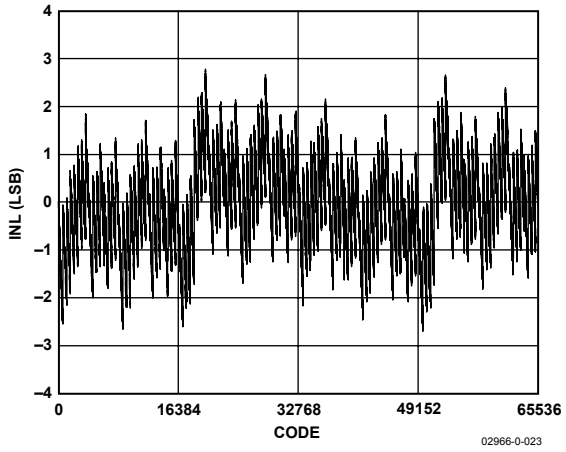

Figure 5. Integral Nonlinearity vs. Code

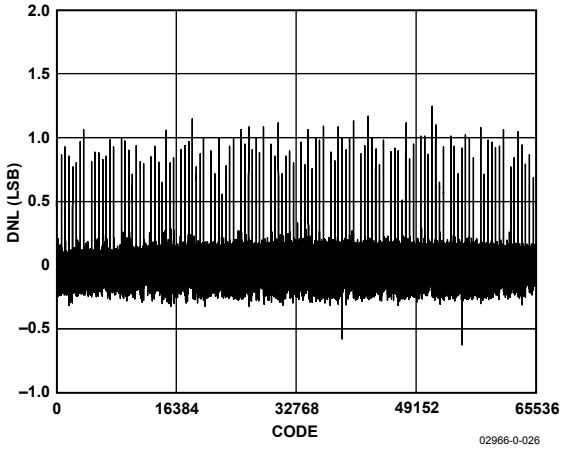

Figure 8. Differential Nonlinearity vs. Code

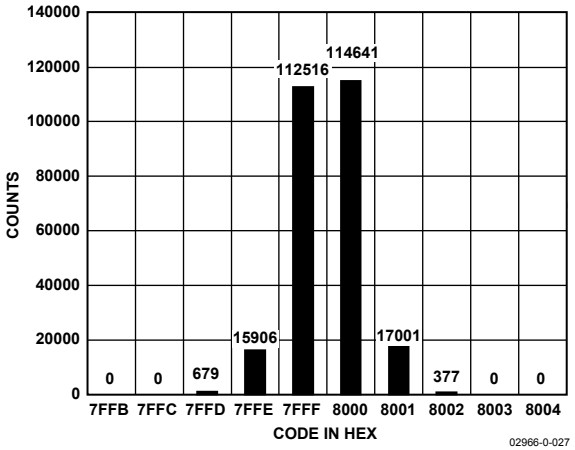

Figure 6. Histogram of 261,120 Conversions of a DC Input at the Code Transition

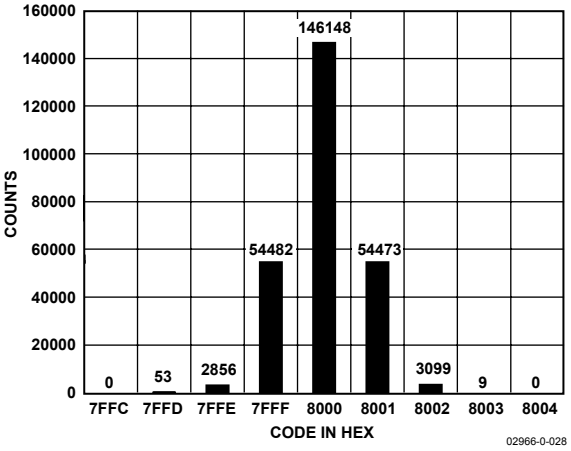

Figure 9. Histogram of 261,120 Conversions of a DC Input at the Code Center

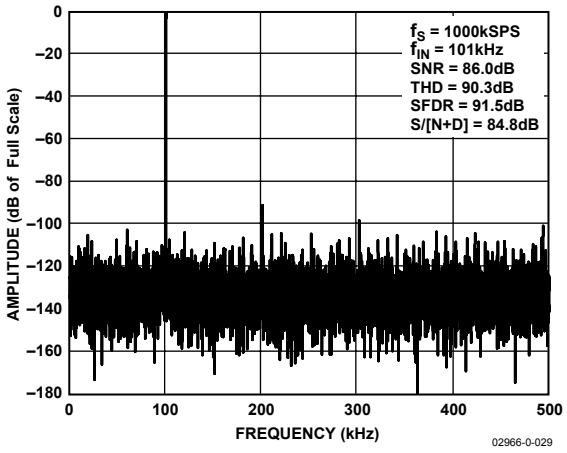

Figure 7. FFT Plot

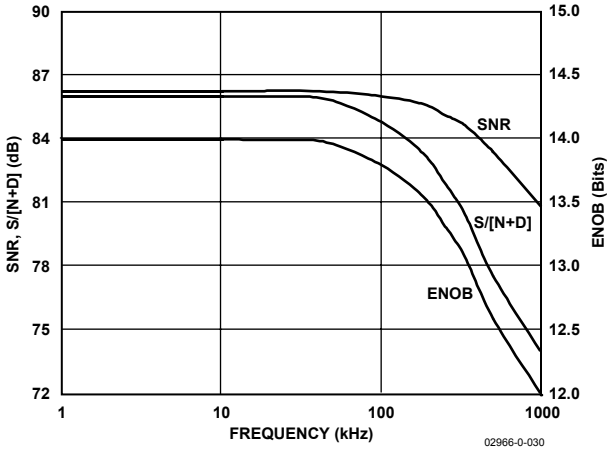

Figure 10. SNR, S/(N+D), and ENOB vs. Frequency

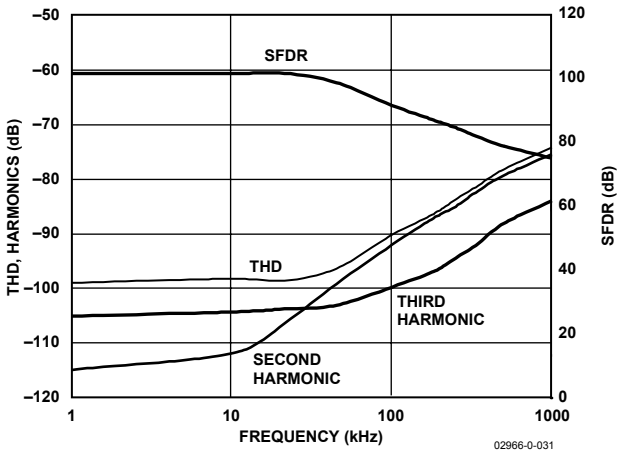

Figure 11. THD, Harmonics, and SFDR vs. Frequency

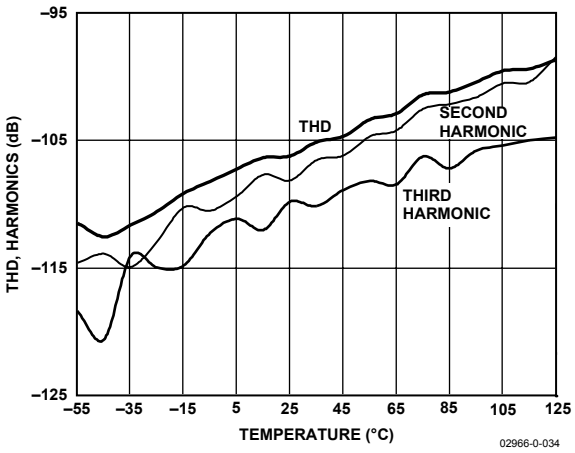

Figure 14. THD and Harmonics vs. Temperature

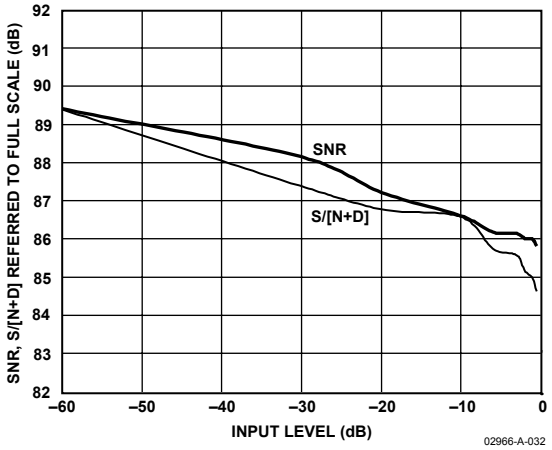

Figure 12. SNR and S/(N+D) vs. Input Level (Referred to Full Scale)

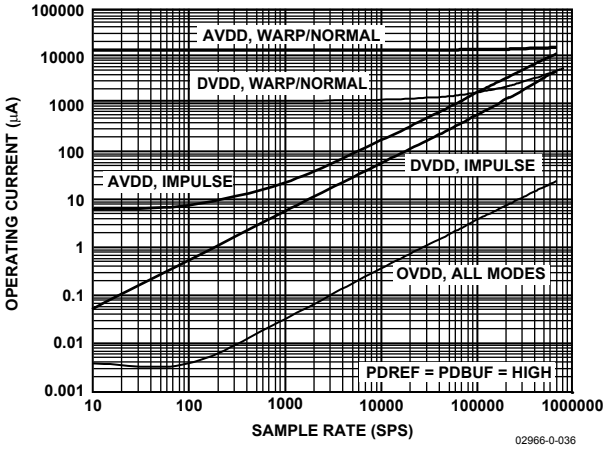

Figure 15. Operating Current vs. Sample Rate

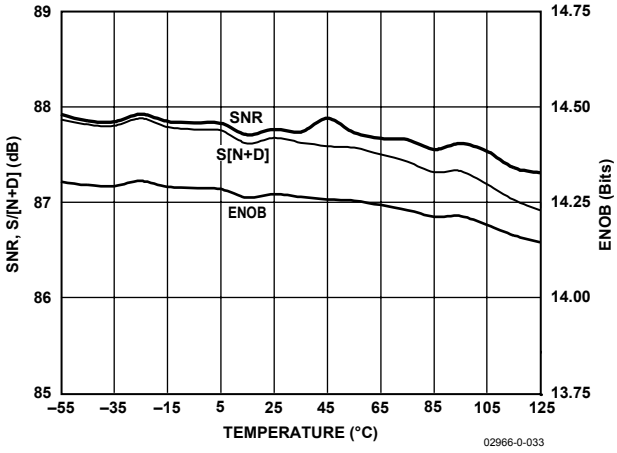

Figure 13. SNR, S/(N+D), and ENOB vs. Temperature

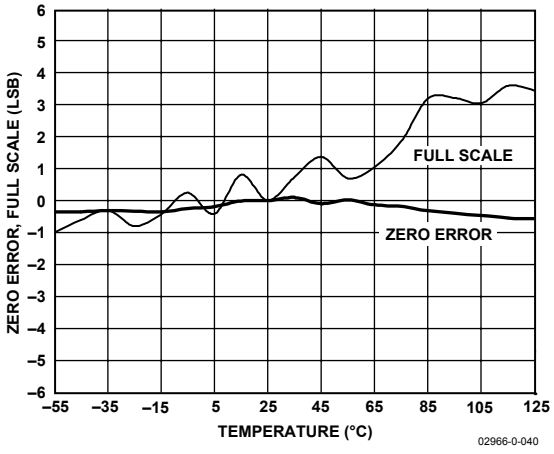

Figure 16. Zero Error, Full Scale with Reference vs. Temperature

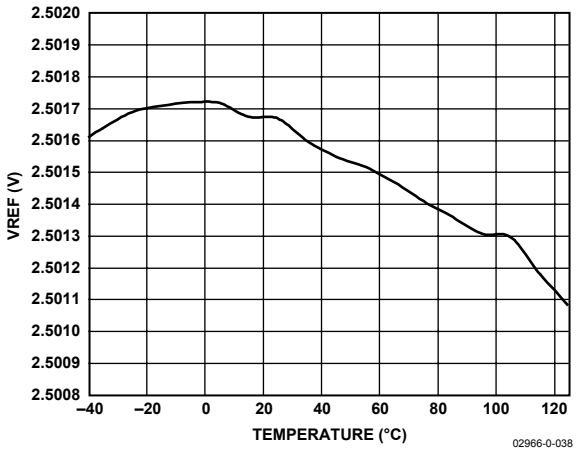

Figure 17. Typical Reference Output Voltage vs. Temperature

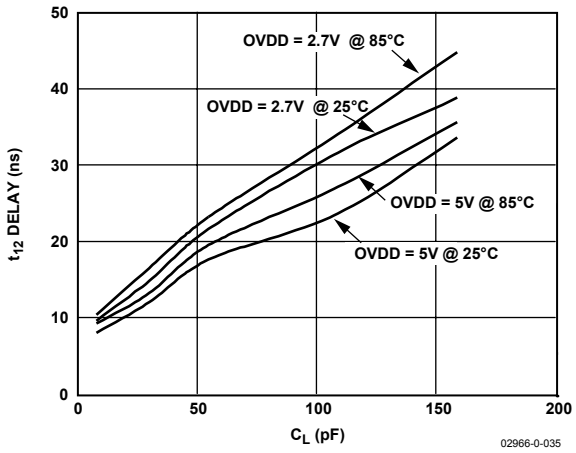

Figure 19. Typical Delay vs. Load Capacitance C_L

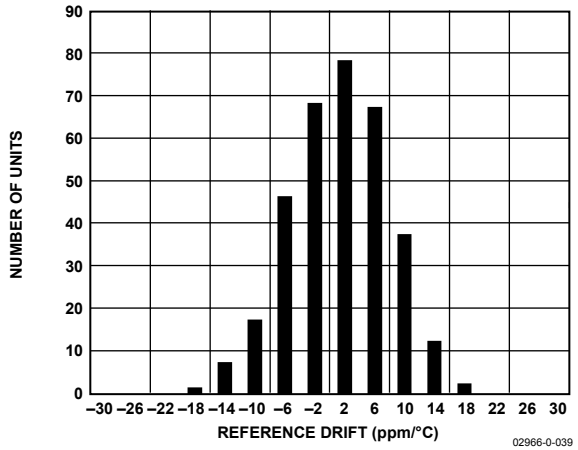

Figure 18. Reference Voltage Temperature Coefficient Distribution (335 Units)