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A completely flexible organic transistor obtained by a one-mask photolithographic process

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A one-mask optolithographic process is proposed for obtaining a completely flexible organic thin-film transistor structure. The proposed device consists in a ''bottom structure'' assembled on a flexible and transparent insulating layer, without any substrate, with source and drain contacts on one side and the gate on the opposite side. The main advantage consists in avoiding the presence of a substrate as the insulator itself is able to support the whole structure. Furthermore, being optically transparent, the insulator is suitable to be employed for the photolithographic realization of the contacts with a one-mask process with no need of mask alignment between source–drain contacts and gate. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1577216]

Organic field-effect transistors have been of great interest due to the fact that they represent the building blocks of electronic systems based on flexible, large-area substrates.[1] The potential market for such applications is great, and this has stimulated substantial efforts both in the academic and industrial fields, which in the last decade have resulted in an impressive improvement in terms of performance and efficiency.[2–6]

Basically, all organic and hybrid devices realized so far consist of a thin-film transistor (TFT) structure, made by sandwiching a thin insulator layer between a conductive layer that acts as gate and an organic semiconductor layer where source and drain contacts are realized. Generally, these structures are assembled starting from a substrate (in hybrid devices it consists of heavily doped silicon, while in all-organic devices, generally plastic or glass are used), but not necessarily.[7] A variety of techniques and materials have been proposed so far for obtaining this kind of structure, as reviewed in Ref. 1.

In this letter, we describe how a completely flexible organic TFT (OTFT) has been fabricated: a flexible layer, $<1\ \mu$m thick, works as insulator and, at the same time, as a free-standing surface for device assembling, similarly to that proposed in Ref. 7, but avoiding the inclusion of a substrate during the whole fabrication process. For this reason, it is completely flexible and suitable to be transferred, after the device assembly, on unusual substrates such as, textiles, or it can be used to wrap three-dimensional surfaces.

The basic structure of the device is described in Fig. 1. It consists of a thin insulating film with metal contacts (source–drain and gate) deposited on opposite sides of the insulating film. Finally, by depositing a suitable organic semiconductor on the source–drain side of the film, the complete OTFT structure is obtained. Fabrication steps have been assessed, and this basic schema has been applied to different device geometries and materials for contacts and semiconductors.

As an insulating layer, the core of the structure, we have selected a 900-nm-thick Mylar™ film (Du Pont) that has a dielectric constant close to that of silicon dioxide (3.3) and a good value of dielectric rigidity (10^5 V/cm) that allows one to apply gate voltages high enough (tens of volts) to induce a measurable field effect. In addition, it is transparent to visible and UV light, which is a very important characteristic for the device assembling technique that we have employed.

After adapting the film to a plastic frame (maintained during the whole process), the devices have been prepared by depositing source and drain contacts on one side of the insulating layer, followed by deposition of the gate metal on the opposite side. Both these steps have been made using a standard photolithographic technique and, most important, this was done with a one-mask process. In the first step, metalized Mylar covered with positive photoresist was exposed to UV light through a mask suitably patterned to form source and drain contacts, while in the second step, thanks to the optical transparency of Mylar (also to UV light), each metal contact (obtained in the first step after developing the photoresist and selectively removing the metal) can act as an opaque mask for the gate definition, with no need of further masks and, most important, of mask aligning. This is done by depositing positive photoresist on the opposite side of the Mylar and then exposing it to UV light irradiated through the Mylar itself. After this step, the gate metal was thermally

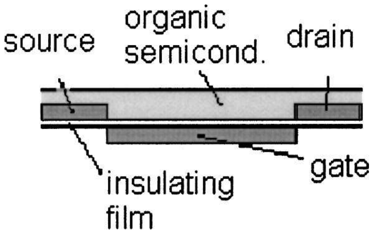

FIG. 1. Structure of the proposed device.

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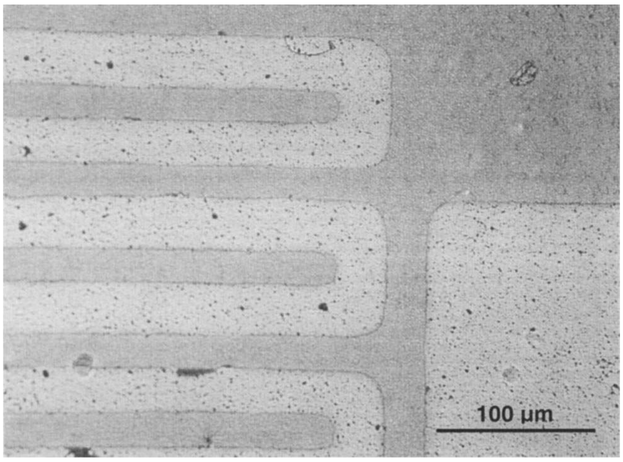

FIG. 2. Detail of the channel area of a device made with a lift-off technique. The picture was taken from the gold-covered side of the film. In order to make the geometry more clearly visible, different metals were used for drain–source (aluminum) and gate (gold) contacts, even if all measured devices were made with all-gold contacts.

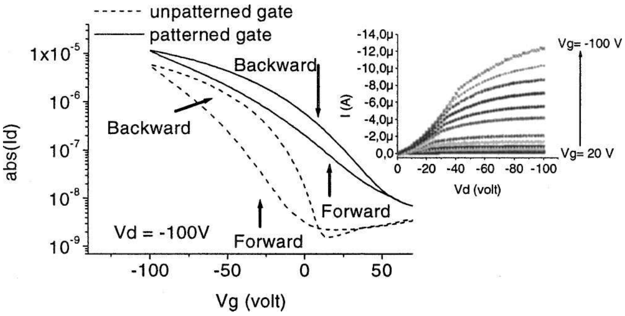

FIG. 3. Comparison between the trans-characteristic curves of a device with unpatterned (dashed line) gate and with a patterned gate (solid line). In the inset, the static output curve on a patterned gate device. All measurements were obtained with a HP4155 semiconductor parameter analyzer.

evaporated on Mylar and finally patterned by a lift-off technique. In this way, the channel area of the device included between source and drain contacts, is precisely gate-covered on the opposite part of the insulator (Fig. 2), thus limiting metal superposition and consequently, parasitic capacitance effects. This technique is therefore particularly simple and could also allow, in a long-term perspective, to obtain more complex circuits, made (as in silicon technology) with several layers of metal and insulator, starting from the two-dimensional patterning of the insulator. With this technique, interdigitated structures with minimum separation between contacts of 20 μm have been obtained. In addition, this same photolithographic process that allowed us to obtain a pattern for metal evaporation can be employed for depositing and patterning contacts made with conductive polymers that can be spin-coated on the photoresist mask and then selectively removed.[8] Work is in progress on this task.

At present, the final active area (i.e., the total area covered by the interdigitated structure) is about 5×10^{-2} cm^2. Another important characteristic of this structure is that, usually, in planar structures, the organic semiconductor is spread all over the surface, therefore allowing unintentional conductive paths between source, drain, and gate that can negatively affect the performance of the device (or, alternatively, requiring a further technological step for ‘‘cleaning’’ the area external to the channel). In our case, as source–drain and gate lie on opposite sides of the insulator, the insulator itself avoids any possible unintentional electrical contact between the gate and the other terminals due to the organic semiconductor.

The basic structure of the TFT includes also the deposition of the organic semiconductor. This can be done with several techniques: spin-coating (OC_1C_{10}-phenylenevinylene devices have been obtained), spraying or, alternatively, by thermal evaporation. All these techniques can be easily employed with the basic structure described.

An example of the measured electrical characteristics is shown in Fig. 3 and refers to a device with interdigitated source and drain contacts, $W/L=3000$, and evaporated pentacene (estimated thickness: tens of nanometers) as an organic semiconductor. In the inset, the I_d versus V_d curves are shown, while the main graphic shows the comparison between the trans-characteristic curves recorded on a structure with a patterned gate contact (solid line) and those recorded on the same sample with the gate made by covering with gold the whole area of source and drain without any patterning of the contact (dashed line). In the first case, any superposition between source–drain and gate contacts is avoided; as a consequence, parasitic capacitance effects are strongly reduced, as can be clearly evinced from the strong (and permanent) reduction of the hysteretic effect shown by the curve in this case. Residual hysteresis can be interpreted both in terms of border effects (higher in interdigitated structures) and with trapping charge effects in the semiconductor.[9–11] Instead, other significant differences observable in the two curves (e.g., drain current intensity and threshold voltage variations) cannot be univocally interpreted since variations of these parameters have also been observed in measurements taken in different days or in samples maintained in an oxygen-free atmosphere. The average values of the electronic parameters, recorded on several devices, are the following: the mobility value of pentacene, deduced from the trans-characteristic curves of the devices taken in saturation and in the linear regime is in the range of 10^{-4} cm^2/V s, Ion/Ioff ratios were up to 2×10^3, and threshold voltages were positive values around 10 V.

Several factors can be varied to improve the structure performances besides, obviously, selecting semiconductors with higher mobility.[12–14] As an example, in this case, the insulating layer is almost a factor of 10 thicker than, for example, typical silicon dioxide layers. Thinner (but still mechanically stable) insulating layers and/or higher values of the dielectric constant could allow a substantial improvement of the transistor characteristics because of the higher value of the insulator capacitance. Furthermore, device geometries with higher W/L ratios could also be realized.

In conclusion, a completely flexible structure for organic field-effect transistors can be easily obtained with a simple one-mask photolithographic technique that allows one to improve device performance through the elimination of parasitic capacitance effects due to metal superposition between source–drain and gate contacts. This technique can be applied to hybrid (metal contacts and organic semiconductors) as well as to all-polymer devices and with a variety of techniques for depositing the organic semiconductor. The complete flexibility of the obtained structure opens up possibilities for innovative electronic applications aiming to employ flexible substrates (as, e.g., textiles or thick plastic films) or to three-dimensional object covering. Present performance, comparable with other already assessed structures, could be further optimized by improving the insulator layer features and the organic semiconductor properties.

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