

A Charge-Modulated FET for Detection of Biomolecular Processes: Conception, Modeling, and Simulation

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Abstract—A novel, solid-state sensor for charge detection in biomolecular processes is proposed. The device, called charge-modulated field-effect transistor, is compatible with a standard CMOS process, thus allowing fully electronic readout and large scale of integration of biosensors on a single chip. The detection mechanism is based on the field-effect modulation induced by electric charge changes related to the bioprocess. A model of the device was developed, to provide a manageable relationship between its output and geometric, design and process parameters. Extensive two- and three-dimensional simulations of the proposed structure validated the model and the working principle.

Index Terms—Charge sensor, DNA detection, DNA-chip, field-effect transistor (FET) sensor, micro-arrays.

I. INTRODUCTION

THERE is a growing interest in solid-state biosensors able to detect biomolecular processes (such as DNA hybridization) that can be fully integrated in a standard CMOS process. Typical techniques for DNA hybridization detection, in fact, usually require the use of bulky and costly lab equipments needed to detect fluorescent, chemiluminescent, or radioactive labels [1], [2]. These optical (or optical-like) indirect methods detect a signal coming from a label attached to the DNA fragment rather than from the fragment itself. In this way 1) a labeling step is needed before measurement, 2) the instrumentation is not portable, so *in situ* measures or portable/disposable detectors cannot be realized, moreover 3) image processing techniques have to be applied for automatic detection. Direct methods such as mass spectrometry [3] [quartz crystal micro-balance (QCM)] avoid the labeling step but still require external components which cannot be easily integrated in a standard process. Finally, most advanced devices based on cantilevers [4] are realized with MEMS, so they require extra steps which increase the cost and decrease the yield.

For these reasons, several new biosensors have been proposed in the last decade, capable of direct electronic readout of the

sensor's output. Direct electronic detection, in fact, seems to be the most promising approach [5] for the realization of simple, portable, inexpensive detection platforms.

II. RELATED WORKS AND MOTIVATION

Electronic detection of DNA is based on a proper transduction of the presence of the target molecule into an electric signal (current, voltage, or charge). In many devices of this kind [5], the selected signal is an electric current flowing through two electrodes. This current may flow through nanoparticles bound to the DNA strand [6], [7], or may be originated by a redox-cycle mediated by redox-active molecules [8], [9], or by an enzymatic reaction [10], [11]. These approaches are indirect methods, as well, since they detect a signal originated by labels bound to the fragment of DNA. Moreover, they are difficult to integrate, since the readout scheme becomes rapidly challenging when hundreds of electrodes are required. A fully electronic DNA sensor was proposed in [12]; in this paper, the problem of the readout scheme was solved by integrating electronics in the silicon substrate, however, the device is not fully compatible with a CMOS process since it makes use of gold electrodes and the transduction mechanism is based on a redox-cycle so, again, a labeling step is needed.

Direct methods based on detection of the intrinsic molecular charge have been proposed, recently. Among them, some are based on an impedance measure such as in [13], others on field-effect measurements by means of capacitances [14], [15], diodes [16] or transistors [17], [18]. These new techniques share the advantage of a direct electronic readout and label-free detection. The main drawback is the need for reference counter-electrodes (usually made of Ag/AgCl) which cannot be easily integrated in a standard CMOS process thus preventing the realization of really low-cost, disposable devices. These electrodes are needed to set the voltage drop between the solution containing the molecules and the substrate and are shared by all the sensors on the chip. A FET-type detector without such electrode is proposed in [19], but in this case a nonstandard CMOS process is needed to ensure proper activation of the transistor.

In this paper, we propose a solid state device able to detect changes of electric charge in the range a few electrons per nanometer² with no need for any external component. Each sensor has an individual, incorporated reference electrode that can be used to set the operating point regardless of other sensors. The device can be realized in standard CMOS technology, providing low-cost, large-scale-of-integration capabilities. The device was modeled and extensively simulated to characterize

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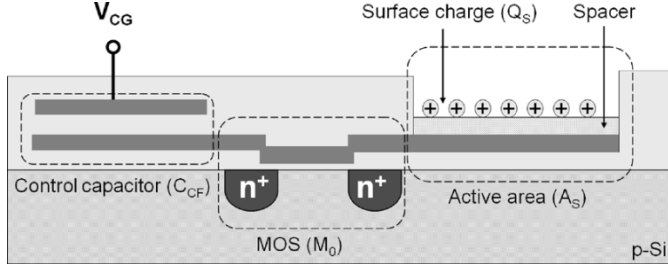


Fig. 1. Proposed device, composed by a floating-gate transistor with a control-gate and an active area.

its behavior with respect to design and process parameters such as geometries, intralayer capacitances, and so on. The model was validated by means of two-dimensional (2-D) and three-dimensional (3-D) simulations which proved the feasibility of the approach.

III. CHARGE-MODULATED FIELD-EFFECT TRANSISTOR (CMFET)

A. Device Structure

The proposed device, that we call charge-modulated field-effect transistor (CMFET), is based on an evolution of the floating-gate MOS transistor. A cross section of the sensor is shown in Fig. 1: it is made-up of a floating-gate transistor (M_0), a control-gate with the role of reference electrode (V_{CG}) and an active area activated by charge induction (A_S).

Through a standard pad opening in the SiO_2 passivation, the floating-gate surface is reached. A thin insulator (spacer) is deposited on top of the exposed floating-gate surface and the charge to be sensed must be (chemically) bound on top of the same spacer. The spacer must be properly chosen to immobilize the charge to be sensed (see Section IV). The control-capacitor and the active area, together, determine the actual voltage difference V_{FG} between floating-gate and silicon bulk so they determine the drain current of the MOSFET transistor. The final voltage is due to the superposition of the effect of each source. If the active area were not present, the entire structure would just simplify to a standard floating-gate transistor. Taking into account the effect of the control-capacitor, the device can be modeled as a standard MOSFET with a modified threshold voltage. Modification of the threshold voltage depends upon capacitive coupling between control-gate and floating-gate and electrical charges trapped into the floating plane in the manufacturing process or by intentional injection/removal (Flash memories).

Let us now examine the role of the active area A_S . If the control-capacitor were not present the structure would behave as predicted by electrostatic laws of induction. The bound surface charge (Q_S) generates an electric field, which causes charge separation inside the buried polysilicon layer [20]. A charge Q_i is induced on the top side of the floating-gate and, since total charge in the buried gate must remain constant, an opposite charge $-Q_i$ appears on the bottom side. As a consequence, charge carriers will be attracted or repelled (depending on silicon doping and Q_S charge sign) underneath the active area. Thus, an electric field and, consequently, a voltage drop (V_{FG})

are generated between silicon substrate and floating-gate. The resulting voltage V_{FG} may activate the MOS transistor (M_0) and determine its drain current. Of course, if the bulk is p-type and the surface bound charge Q_S is positive the native MOS transistor M_0 could be turned-on since the voltage drop V_{FG} would be positive; on the contrary, if the bound charge is negative the MOS transistor could not be turned on because of the negative sign of V_{FG} . The contrary is true in case of n-doped bulk.

In the device of Fig. 1, the two mechanisms concurrently set the floating-gate voltage V_{FG} with respect to the silicon body. A relationship between the surface charge Q_S , the control-gate voltage V_{CG} and the floating-gate voltage V_{FG} stems from charge conservation principle: since the floating-gate is isolated, its charge must remain constant, unless an injection mechanism intervenes. Control- and floating-gate realize a plane, linear, poly1-poly2 capacitor (C_{CF}), whose capacitance depends upon oxide thickness (t_{P1P2}) and gate area (A_{CG}). A second, parasitic, capacitor (C_{FB}) is formed by floating-gate and silicon body. This latter capacitor is not linear and its value slightly depends on floating-gate voltage, but can be considered constant if the device is completely turned on, i.e., if the floating-gate voltage is higher than the threshold voltage of the MOS transistor. In standard CMOS processes, the second capacitor (the bottom-plate parasitic capacitor) is usually around a 10%–20% of the first one.

The charge conservation principle states that total charge into the insulated floating-gate must remain constant. Writing all charges in terms of capacitances we obtain (all voltages are expressed with respect to silicon body voltage)

$$Q_{F0} = Q_i(Q_S) + Q_{CCF} + Q_{CFB} \\ = Q_i(Q_S) + C_{CF}(V_{FG} - V_{CG}) + C_{FB}V_{FG} \quad (1)$$

$$V_{FG} = \frac{C_{CF}}{C_{CF} + C_{FB}}V_{CG} + \frac{Q_{F0} - Q_i(Q_S)}{C_{CF} + C_{FB}} \quad (2)$$

where Q_{F0} is total charge trapped inside the floating gate (this charge can slightly change along different devices and depends upon the manufacturing process) and Q_i is the charge induced on polysilicon surface by the surface charge Q_S . Equation (2) represents the relationship between floating-gate voltage, control-voltage and surface charge. So, drain current of the MOS transistor M_0 is determined by both control-voltage V_{CG} and surface charge Q_S .

As usually done in floating-gate transistors, the effect of the different sources is modeled as a change of the effective threshold voltage (V_{THF}) of the MOS transistor. It can be shown that the surface charge bound on top of the active area modulates the threshold voltage of the transistor. Equation (3) shows this relationship

$$V_{FG} - V_{TH} = V_{CG} - V_{THF} \\ = \frac{C_{CF}}{C_{CF} + C_{FB}}V_{CG} \\ + \frac{Q_{F0} - Q_i(Q_S)}{C_{CF} + C_{FB}} - V_{TH} \\ \simeq V_{CG} - \left(V_{TH} - \frac{Q_{F0} - Q_i(Q_S)}{C_{CF} + C_{FB}} \right) \\ V_{THF} \simeq V_{TH} - \frac{Q_{F0} - Q_i(Q_S)}{C_{CF} + C_{FB}}. \quad (3)$$

The above simplification is possible if $C_{CF} \gg C_{FB}$. In this way, thanks to control-capacitor C_{CF} and the reference electrode V_{CG} , both positive and negative charges can be sensed, regardless of the doping of the bulk and type of the transistor. A positive charge Q_S will result in a negative shift of the effective threshold voltage, while a negative charge will produce a positive shift of threshold (for a n-type MOS transistor, the contrary is true for a p-type).

B. First-Order Model

Equations (2) and (3), predict the behavior of the device, once Q_i is known. To obtain a manageable relationship between effective threshold voltage V_{THF} and surface charge Q_S , induced charge Q_i must be identified. The floating-gate voltage is determined by the control-voltage and the surface charge: the two sources are independent and their effect must sum up to produce the final result. The general expression for floating-gate voltage must be

$$V_{FG} = f_1(V_{CG}, t_{P1P2}, t_{OX}, \epsilon_{OX}, A_{CF}, P_{CF}) + f_2(Q_S, t_{SP}, \epsilon_{SP}). \quad (4)$$

Function $f_1()$ was found previously ((2)) and stems from capacitive coupling between control capacitor and floating-gate capacitor. This function is linear and depends upon process parameters (field oxide thickness t_{OX} , poly1-poly2 oxide thickness t_{P1P2}), physical values (ϵ_{OX}) and geometric parameters (control-gate area A_{CF} and perimeter P_{CF} as well as active area A_S and perimeter P_S). Function $f_2()$ should be determined by simulation and will surely depend upon the distance between the net surface charge and the floating-gate plate (spacer thickness t_{SP}) and the dielectric constant of the spacer material (ϵ_{SP}).

A first-order model simplification suggests that, if the spacer thickness (t_{SP}) is much thinner than other dimensions, the hypothesis of perfect induction is plausible. In this case, the induced charge Q_i would be equal in magnitude and opposite in sign to the sensing charge Q_S

$$Q_i = -Q_S. \quad (5)$$

If (5) holds, function $f_2()$ can be directly obtained from (2) simply substituting the value of Q_i . Thus, we have

$$f_1(V_{CG}, t_{P1P2}, t_{OX}, \epsilon_{OX}, A_{C1}, P_{C1}) = \frac{C_{CF}}{C_{CF} + C_{FB}} V_{CG} \quad (6)$$

$$f_2(Q_S, t_{SP}, \epsilon_{SP}) = \frac{Q_{F0} + Q_S}{C_{C1} + C_{FB}} \quad (7)$$

$$C_{CF} = \frac{A_{CF}\epsilon_{OX}}{t_{P1P2}} + C_{fringe} P_{CF} \quad (8)$$

$$C_{FB} = \frac{A_{CF}\epsilon_{OX}}{t_{OX}} + \frac{A_S\epsilon_{OX}}{t_{OX}} \quad (9)$$

where the meaning of each parameter is given in Table I.

In case of perfect induction, floating-gate voltage linearly depends upon control-gate voltage and sensing charge Q_S . Applying the same manipulation of (3), we obtain the effective threshold voltage as a linear function of Q_S and V_{TH}

$$V_{THF} \simeq V_{TH} - \frac{Q_{F0} + Q_S}{C_{CF} + C_{FB}}. \quad (10)$$

TABLE I
GEOMETRIC AND PROCESS PARAMETERS

Parameter	Meaning	Units
C_{CF}	Capacitance of the control capacitor	F
C_{FB}	Capacitance between floating gate and silicon body	F
Q_{F0}	Electric charge trapped in the floating gate	C
C_{fringe}	Fringe effect of the control capacitor	F/m
t_{P1P2}	Oxide thickness between poly1 and poly2	m
A_{CF}	Area of the control capacitor	m²
P_{CF}	Perimeter of the control capacitor	m
A_S	Area of the active-area	m²

The amount of electric charge immobilized on the surface of the active area modulates the effective threshold voltage (V_{THF}) of the transistor. The threshold voltage can be electrically measured by sensing the drain current for a given control-gate voltage, or, alternatively, by detecting the control-gate voltage for a constant drain current.

IV. BIOMOLECULAR CMFET SENSOR

A. Working Principle

The biomolecular sensor is based on the use of the CMFET transistor to detect the negative electric charge associated to oligonucleotides. The sensor is composed of a CMFET with one control-gate and an active area functionalized with a proper sandwich of a spacer material and single-strand oligonucleotides, providing the sensing charge (Q_S).

The electric charge of oligonucleotides on the surface of the active area will change the effective threshold voltage of the transistor as predicted by (10). The control-gate can be used to set the operating point of the device, zeroing the effect of unknown charge Q_{F0} . The key point is the ability to immobilize the single-strand oligos on the surface of active area so that the device can sense their negative charge (on this subject see Section IV-B).

Hybridization will cause the net surface charge to double as the complementary strand sticks to the immobilized oligo. A change in the surface charge will further increase the effective threshold voltage. In fact, if Q_{DNA1} is the charge of the immobilized single strand, and Q_{DNA2} is the charge of complementary hybridized strand, the change of effective threshold voltage after hybridization is given by (11)

$$\Delta V_{THF} \simeq - \frac{Q_{DNA2}}{C_{CF} + C_{FB}} \quad (11)$$

$$V_{THF2} \simeq V_{THF1} - \frac{Q_{DNA2}}{C_{CF} + C_{FB}}. \quad (12)$$

Properly choosing the control voltage and geometric parameters, the designer can set this final change to raise the effective threshold above the supply voltage, thus preventing the transistor from conduction. In this way, the presence of complementary strands will generate an on/off digital signal easily detected by underlying electronics.

The whole mechanism is depicted in Fig. 2 that shows how hybridization can be detected by detecting the charge induced on the floating-gate.

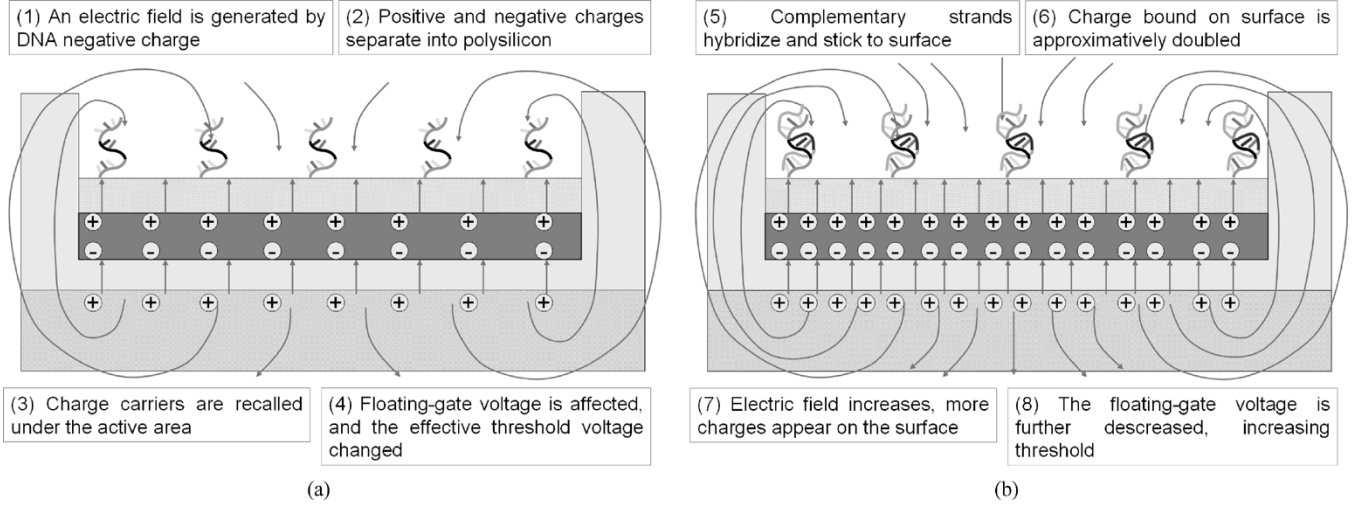


Fig. 2. Hybridization detection. (a) Single-strand target oligonucleotides. (b) Resulting double-strand after hybridization with the probe.

B. Surface Functionalization

To activate the surface, a layer of properly functionalized spacer molecules must be covalently linked to the underlying surface. Depending on the surface material (oxides or metals), functionalization with silane-terminated or thiol-terminated molecules can be made [21], [22], [7]. In our case, the surface material is aluminum oxide (or another oxide), therefore silane-terminated molecules must be used. The second step consists in anchoring the DNA strands to the spacer layer. This can be done by chemically modifying the DNA strands with a proper side group. As an example, if the spacer molecules (silane-terminated) bear a thiol group, a thiol-modified DNA strand can be linked to this, therefore obtaining a close-packed layer of DNA strands strongly anchored to the sensor surface.

V. SIMULATIONS

A. Device Physics

The determination of function $f_2()$ in (3), and its dependence upon geometric and process parameters requires the identification of the relationship between floating-gate voltage V_{FG} (the unknown quantity) and the bound electric charge Q_S (the source). To do this we have to solve a typical electrostatic problem since we must find the voltage on a conductor (the floating-gate) in a structure made up of conductors and dielectrics. For each conductor (M_h) in the system we know either the voltage (control-gate) or the electric charge (floating-gate). In each point $P(x, y, z)$ of a dielectric we know the dielectric constant $\varepsilon(x, y, z)$ and electric charge density $\rho(x, y, z)$ (e.g., fixed surface charge Q_S). The situation is complicated by the presence of the silicon body which, being a semiconductor, is described by nonlinear equations. Fortunately, the device will be operated only when the MOS transistor is ON and deep in its saturation region of operation. In this condition, the conductive channel under the gate is formed and behaves as a thin metal sheet underlying the silicon surface. For this reason we can treat the silicon body as an equivalent conductor and deal with a quite typical electrostatic problem.

B. Equations and Materials

1) *Dielectrics*: The characteristic equation for each point $P(x, y, z)$ in a dielectric is the Poisson Equation that we write as

$$\nabla^2 V(x, y, z) = -\frac{\rho(x, y, z)}{\varepsilon(x, y, z)} \quad (13)$$

where $V(x, y, z)$ is the electric potential at spatial position $P(x, y, z)$, $\rho(x, y, z)$ is the electric charge density and $\varepsilon(x, y, z)$ is the dielectric constant of the material. Of course, for each point of the structure the dielectric constant may change, if the material changes. In the CMFET sensor, the electric charge density is null everywhere except on top of the spacer material on the active area, so (13) holds on the surface of the active area while everywhere else it degenerates to the Laplace Equation

$$\nabla^2 V(x, y, z) = 0. \quad (14)$$

2) *Conductors*: Inside each conductor the electric field is null, so the potential is constant all over the conductor. Thus, for every point $P(x, y, z)$ of the h -est conductor M_h

$$V(x, y, z) = V_h. \quad (15)$$

Of course, the actual value of V_h is either unknown (for floating conductors) or set by definition (the control-gate voltage). So, inside the conductors (15) holds and the electric charge is null everywhere. Mobile charges (charge carriers) are forced on the surface of the conductor and generate a surface charge density. The external electric field is orthogonal to the conductors surface and is given by the following equation:

$$\vec{E}_{EXT} = \frac{\sigma}{\varepsilon} \vec{n}. \quad (16)$$

Where vector \vec{E}_{EXT} is orthogonal to the surface and directed inside-out the conductor; σ is the surface charge density and ε , of course, dielectric constant of outer material. Equation (16) can be derived from Gauss law and applying the conductor property (electric field is null inside the conductor). Obviously, for isolated conductors (the floating gate), total charge is set and

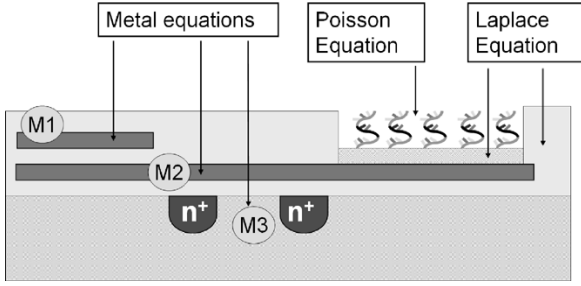


Fig. 3. CMFET biomolecular sensor and different materials and equations: metal equations ((15)–(17)), Poisson equation (13) and Laplace equation (14).

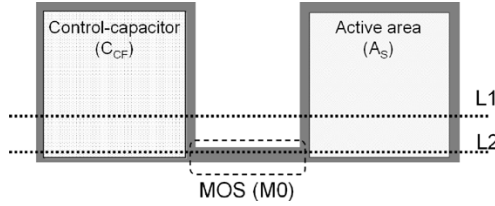


Fig. 4. Top-view of the device. L2 represents cross section position for Fig. 1, while line L1 represents cross section position used for simulation.

cannot change, so the integral of surface charge density calculated all over the surface S_{Mh} of conductor M_h has to be constant

$$\int_{S_{Mh}} \sigma dS = Q_{Mh}. \quad (17)$$

Total charge should be null, even if it can be nonzero in case of a floating conductor, which can collect charge carriers during the manufacturing process. To summarize, Fig. 3 shows, in a pictorial way, a cross section of the device and the different Equations, which describe different materials.

In Fig. 3 the labels M1, M2, and M3 show the three different conductors (control-gate, floating-gate, silicon body) of the structure.

C. Finite Difference Method

1) *Discretization and 2-D Model:* In order to solve the problem we need to solve a system of partial differential equations (PDE). The key point here is the interaction between the two different sources (control-gate and surface charge). The problem is inherently 2-D, so it cannot be solved in closed form with standard methods such as those used for ISFET's [23], [24]. For this reason, we applied the Finite Difference Method (FDM) to transform the differential equations in difference equations. In this way the problem becomes a linear system of equations (the system is linear because we chose to treat silicon body as a conductor) and can be solved applying numerical methods. Given the geometric structure of the device, the third dimension is not essential to understand the sensor functionality. In fact, the two basic structures (the plane control capacitor and the active area) depends prevalently on the vertical electric field. For this reason we concentrate the analysis on the 2-D model represented by the cross section of the device shown in Fig. 1. The floating gate is split in two different areas since, as depicted in Fig. 4, the effective gate area (the area of the floating gate which sits on top of the MOS

transistor) is several orders of magnitude smaller than the area of both active area and control capacitor. Including the gate area in the 2-D model would overestimate its contribution to the final floating-gate voltage. For this reason we treat the floating-gate as two different conductors with the same voltage (short-circuited) rather than one single piece of metal. This concept is clarified in Fig. 4, which shows a top view of the device. Line L2 corresponds to the cross-sections used in Section III-A and in Fig. 1, which take into consideration the MOS transistor, while line L1 corresponds to the cross section used for simulation.

2) *Boundary Condition:* We are interested in solving the problem with respect to voltage differences. Since we are looking for complete determination of functions $f_1()$ and $f_2()$ we need to express all voltages with respect to the silicon bulk voltage. The silicon body belongs to the structure we are investigating, so we cannot apply a boundary condition on it. More generally, we apply Neumann boundary conditions to the frontier of the area containing all the four conductors. We impose that the voltage should be zero at infinity. After discretization of the domain and of (13)–(17) the problem boils down to a linear problem similar to a classic Poisson problem [25] even if slightly complicated by the presence of the floating-gate. It can be shown that the matrix describing the system is a modified penta-diagonal sparse Poisson matrix, with additional rows responsible of modeling the floating conductor [additional rows are generated by discretization of (16) and (17)]. This linear system was solved using a MATLAB tool developed to this purpose.

3) *MATLAB 2-D Simulation Results:* Fig. 5 shows the voltage distribution when the control-gate is set to 5 V and a negative Q_S charge is applied. As predicted in Section III, the voltage drop between floating-gate and silicon surface is modulated by the presence of charge Q_S . The working principle of the CMFET transistor is proved: a sensing charge Q_S put at distance t_{SP} from a floating-gate, generates the electric field and the voltage drop required to drive the transistor. A quantitative estimation of the effect of the charge, as well as the biasing effect of the control-gate is given in Figs. 8–10. Full characterization of the CMFET device requires the identifications of function $f_1()$ and $f_2()$.

Determination of $f_1()$ —Floating-Gate Voltage versus Control-Gate Voltage: Fig. 8 shows the set of simulations used to determine this relationship. In these simulations we kept constant everything except control-gate voltage V_{CG} .

Determination of $f_2()$ —Floating-Gate Voltage versus Electric Charge: If (5) holds, the relationship between floating-gate voltage and the sensing charge has to be linear. To prove this we fixed all parameters except the net electric charge. Fig. 9 shows the result of this set of simulations.

Determination of $f_2()$ —Floating-Gate Voltage versus Spacer Thickness: As shown in Fig. 10, there is a slight change in floating-gate voltage, which increases with an increase of the spacer thickness t_{SP} . This slight dependence can be justified since, increasing the distance between sensing charge and floating gate, the induced charge Q_i should decrease and the floating voltage increase as stated by (2). With an increase of 200% of the spacer thickness, the floating-gate voltage changes

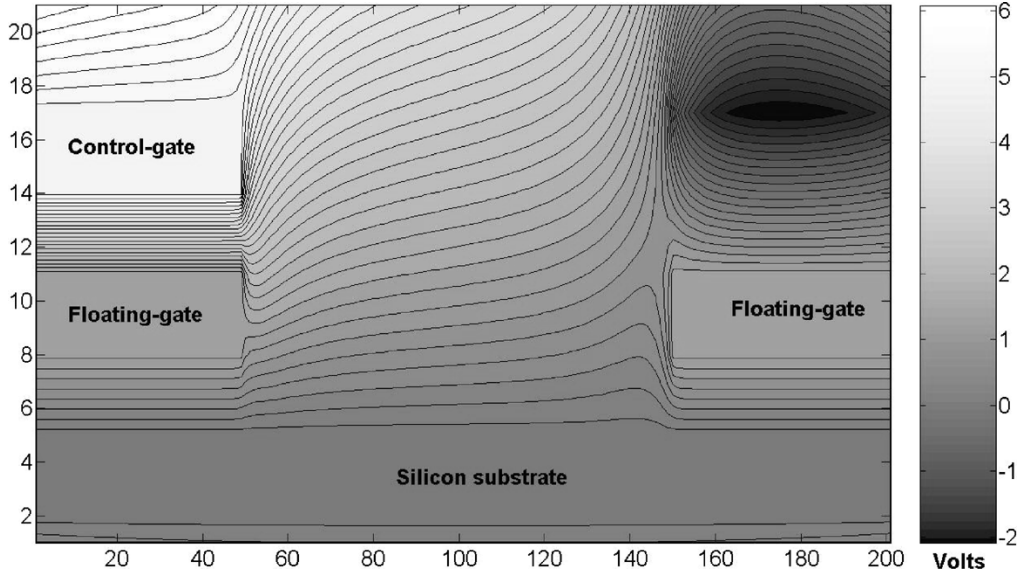


Fig. 5. Voltage contour plot.

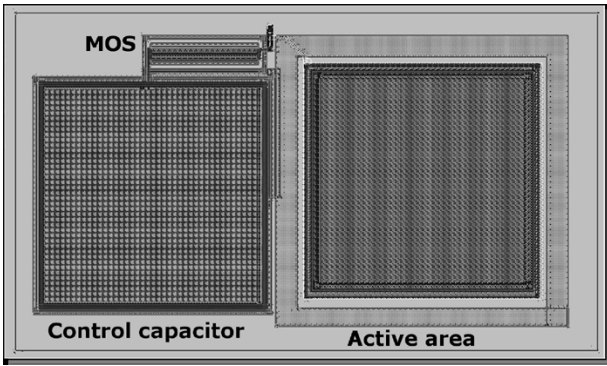


Fig. 6. Mask layout.

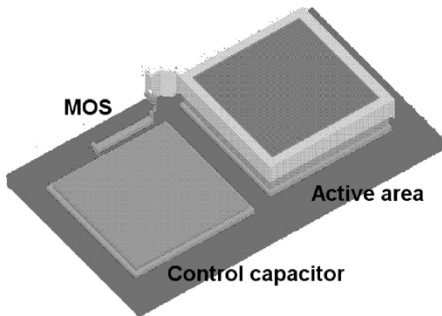
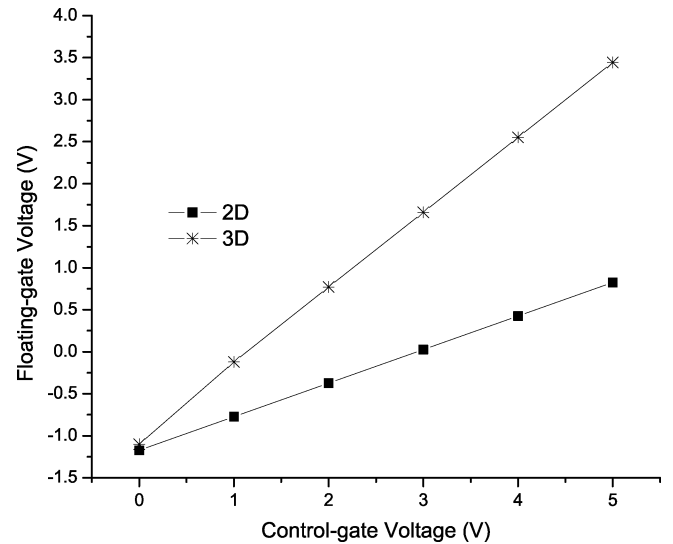


Fig. 7. Solid model: 3-D CMFET structure (passivation removed).

of only about 12%. This result proves that the perfect induction hypothesis, formulated in Section III, is plausible when the spacer thickness is of the same order of magnitude of the oxide thickness. Since we assume that the real spacer thickness of the realized device will be several orders of magnitude smaller than the oxide thickness, we can conclude that the floating-gate voltage does not depend upon spacer thickness. As a result, (5) holds and the effective threshold voltage is correctly predicted by (10).

Fig. 8. Floating-gate voltage versus control-gate voltage. 2-D simulations ($Q_S = -1$ pC, $t_{SP} = 5$ μm) and 3-D simulations ($Q_S = -20$ pC, $t_{SP} = 0.02$ μm).

The theoretical model of Section III is proved by simulations. The relationship between both V_{CG} and Q_S and the floating-gate voltage is linear.

D. 3-D Simulations

1) *Solid Model*: The complete 3-D structure was simulated by means of specialized CAD software (CoventorWare [26]). The Cadence layout editor was used to design the device layout, shown in Fig. 6. The layout was imported into Coventor Designer, converted to a 3-D solid model, shown in Fig. 7, meshed and simulated (Coventor Analyzer). The solid model includes nearly all the different layers and materials of the actual chip.

Process parameters used in simulation come from a CMOS 0.8 μm process from AMS (AustriaMicroSystems) that was chosen as target process for integration.

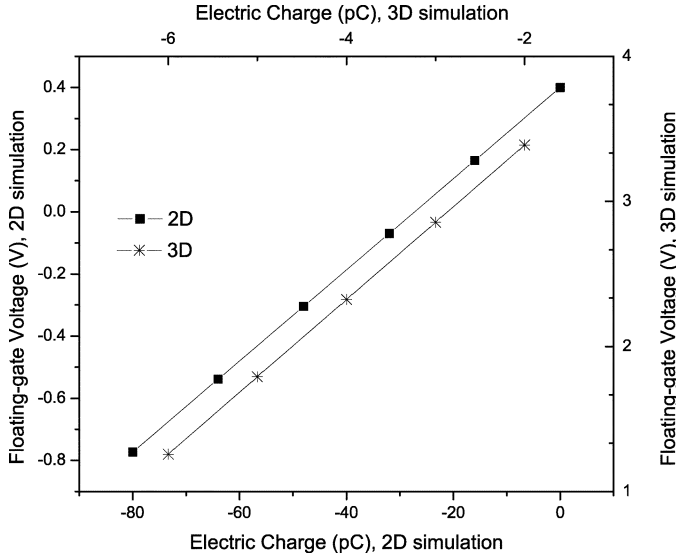


Fig. 9. Floating voltage versus charge density. 2-D simulations ($V_{CG} = 1$ V, $t_{SP} = 5$ μm) and 3-D simulations ($V_{CG} = 5$ V, $t_{SP} = 0.02$ μm). 2-D simulations shown on bottom-left axis and 3-D simulations on top-right axis.

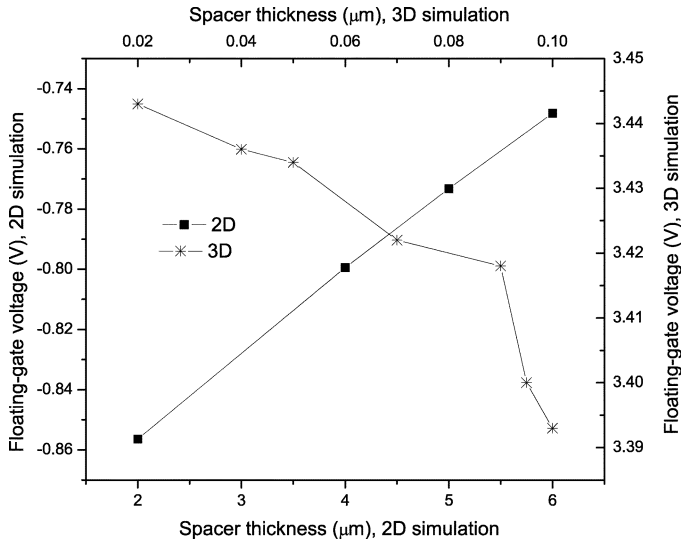


Fig. 10. Floating-gate voltage versus spacer thickness. 2-D simulations ($Q_S = -1$ pC, $V_{CG} = 5$ V) and 3-D simulations ($Q_S = -20$ pC, $V_{CG} = 5$ V). 2-D simulations shown on bottom-left axis and 3-D simulations on top-right axis.

The 3-D simulation takes into account the second order effects of the real structure of the device that could not be included in the 2-D simulations, thus it was helpful for further verification of theoretical results.

2) *CoventorWare 3-D Simulation Results*: Three different sets of simulations were performed in order to determine functions $f_1()$ and $f_2()$. For each simulation set, all parameters were constant except one specific variable swept linearly.

Determination of $f_1()$ —Floating-Gate Voltage versus Control-Gate Voltage: Sweeping variable is the control-gate voltage. Active area is $10\,000$ μm^2 , charge density is equal to $2fC/\mu\text{m}^2$, spacer thickness is 0.02 μm . Fig. 10 shows the linear relationship between floating- and control-voltage.

Determination of $f_2()$ —Floating-Gate Voltage versus Electric Charge: Sweeping variable is the net electric charge.

TABLE II
COMPARISON BETWEEN SIMULATION RESULTS (SIM) AND PREDICTIONS (PRED) MADE WITH THE FIRST-ORDER MODEL OF (6)–(9)

Area [$\mu\text{m} \times \mu\text{m}$]	α_1	α_1	ε_{r1} [V/V]	α_2	α_2	ε_{r2} [V/V]
	PRED [V/V]	SIM [V/V]		PRED [mV/pC]	SIM [mV/pC]	
100x100	0.928	0.891	4.15%	52.3	52.5	0.38%
80X80	0.940	0.904	3.98%	53.6	53.2	0.75%
60X60	0.950	0.914	3.94%	54.7	53.8	1.67%
40X40	0.962	0.922	4.34%	55.5	54.4	2.02%

Active area is $10\,000$ μm^2 , control-gate voltage is equal 5 V, spacer thickness is 0.02 μm . Fig. 9 shows the linear relationship between floating- and sensing electric charge.

Determination of $f_2()$ —Floating-Gate Voltage versus Spacer Thickness: Sweeping variable is spacer thickness t_{SP} . Active area is $10\,000$ μm^2 , control-gate voltage is equal 5 V, charge density is $-2fC/\mu\text{m}^2$. Fig. 10 shows that floating-gate voltage, in the 3-D case, is even less dependent from spacer thickness. The difference in the slope of the 2-D and 3-D curves is probably due to the fact that the 3-D curve is on a much more compact scale than the 2-D curve. Moreover, the 3-D simulation could be scaled to much thinner spacers (tens of nanometers). In this case the changes probably depend more on numeric errors than on a real field-effect.

The first-order model described in Section III predicts that the actual floating-gate voltage should depend linearly both on control-gate voltage and on sensing charge. Under the perfect induction hypothesis, functions $f_1()$ and $f_2()$ should reduce to a linear proportionality expressed by parameters α_1 and α_2 :

$$f_1() = \alpha_1 V_{CG} \quad (18)$$

$$f_2() = \alpha_2 Q_S \quad (19)$$

where α_1 and α_2 depend upon process and geometric parameters of Table I under the assumption of $Q_{F0} = 0$. For the preceding set of simulations the extrapolated (simulated) values of α_1 and α_1 were compared with the values predicted applying (6)–(9). The results are shown in Table II, altogether with the relative error between simulation and model prediction, and prove that the first-order model is reliable and can be used to predict the behavior of the device just using process parameters and geometric layout information, without the need of further 3-D or 2-D simulations.

VI. DISCUSSION

A. Sensitivity

Sensitivity of the proposed CMFET device can be derived from Table II which was computed for a 0.8 μm CMOS process from AustriaMicroSystems (AMS). For an active area of 40 $\mu\text{m} \times 40$ μm (row 4 in Table II), the predicted α_2 linear coefficient for the CMFET sensor is $5.44E10$ (V/C). In this case, a charge distribution of only one electron charge per μm^2 would cause a voltage shift of 14 μV . A quantitative comparison with standard, commercial fluorescent techniques for hybridization detection is possible, since it has been estimated [27]–[29] that, with the fluorescent approach, the minimum detectable amount of DNA molecules is on the order of 10^7 . The charge associated to such amount of molecules (electric charge of the

DNA double strand is $2e^-$ per base pair [30]) is expected to cause a voltage shift that can be roughly estimated as being on the order of hundreds of millivolts (Table II).

B. Comparison With Related Works

With respect to many other sensors for hybridization detection, the CMFET is attractive for its extreme simplicity. It allows direct detection of hybridization process, with no need for complex, additional process steps. For this reason it allows the realization of highly integrated arrays with thousands of active sites, direct detection and fully electronic readout capabilities. The electronic readout is also attractive for the possibility of implementing portable and/or disposable medical kits.

With respect to other devices developed to the purpose of detecting an electric charge (such as the ISFET, CHEMFET and their derivatives [14], [19], [31]–[33]), the CMFET sensor has the advantage of being completely integrated in a standard CMOS process. There is no need for an external reference electrode since the capability to turn-on the FET transistor is due to the presence of the integrated control-electrode V_{CG} capacitively coupled to the floating-gate MOS transistor. In such a way, the detection mechanism is triggered by *differences* in the effective threshold voltage and not by absolute values. The charge to be sensed causes shifts in the threshold voltage so, any static contribution to total charge (such as the charge trapped in the floating metal and the double layer due to surface/liquid interface) can be automatically canceled.

A possible crucial point of this device is a proper balance between sensitivity and selectivity, as the device can be made (with a proper design) extremely charge sensitive, and detect every kind of charge variation. Therefore, double layer perturbation [34] can be a problem. Anyway, if DNA target strands are dense enough on the surface, they form a close packed layer and the double layer should not form (or form partially) on the surface of the insulating layer (see Section IV-B). On the other hand, if there is a contribution of the double layer, this should not be perturbed by the hybridization, provided that the ionic strength of the solution where both target and probe strands are merged does not change. So, differential measurements can be made, probing the effect on the device (with target strands) of a ionic solution of same ionic strength without probe strands.

The integration of the reference electrode within each sensor is particularly interesting for what concern electronic readout. In fact, a reference electrode is needed in any readout circuitry implementing feedback or CDS (correlated double sampling) techniques. A standard counter electrode in solution would be shared among all sensors, thus slowing the response of the system (the feedback loop would involve the solution and its relatively slow kinetics). When each sensor has a different reference electrode, the feedback involves only MOS devices.

VII. CONCLUSION

A novel solid-state sensor for direct charge detection in biomolecular process is proposed. The sensor allows charge detection in a fully integrated CMOS process without external components and electrodes. Proposed application is DNA hybridization detection, but the same device can be used for

detection of any biomolecular process involving a change in electric charge (antigene/antibody interaction, proteomics). A first-order model of the device, based on solid-state silicon structure and CMOS process, was developed. A set of Equations relating the sensor's output to design parameters (such as geometries and layout masks) and process parameters (such as electron mobility, field and gate oxide thickness, metal-metal or poly poly capacitances) was provided and validated by 2-D and 3-D simulations. CMOS compatibility paves the way to integration of thousands of sensor sites on a single chip, with fully electronic readout capability.

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